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Comparisonof Electrical Performance andStability of Flexible CarbonNanotube Thin Film Transistorsof Different Gate Structures

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Abstract: In this work, fabrication of top, bottom and dual-gate carbon nanotube thin film transistors (CNTTFTs) of different dimensions with single-walled carbon nanotubes (SWCNTs) of99.99% semiconducting purity on a polyimide substrate are reported. Electrical performance comparison of flexible CNTTFTs with different gate structures located at the top, bottom and both at the top and the bottom(dual-gate) of the SWCNTs thin film used as a channel isstudied.Top, bottom, and dual-gate CNTTFTs exhibited p-type behavior. Dual-gate CNTTFTs outperformed the bottom–gate and top-gate CNTTFTs of identical dimensions in on-off current ratio, transconductance, drain conductance, subthreshold slope and mobility. Dual-gate and top-gate CNTTFTs exhibited athreshold shift of less than 1.3V and stability in other electrical performance parameters other than threshold voltage without muchvariation over a time of 60 days exposed to air after fabrication. This work demonstrates that dual-gate CNTTFTs have exhibited better electrical performances and gate control over the channel than the top-gate and bottom-gate CNTTFTs. Dual-gate CNTTFTs are preferred for better electrical performances than top-gate and bottom-gate in flexible applications.
Keywords: Carbon nanotube thin film transistors,dual gate, flexible, on-off current ratio, single-walled carbon nanotubes.

Introduction

Single-walled carbon nanotubes (SWCNTs) in the form of thin-film are used in the channel area of carbon nanotube thin film transistors (CNTTFTs). SWCNTs exhibit high carrier mobility, low operating voltage and are available in solution forms [1-4]. CNTTFTs are fabricated on a wafer scale on silicon (Si) substrates, and electrical performances were studied [5-10]. The researchers are using SWCNTs of higher semiconducting purity, the higher density of deposition and orientation of random or aligned in the fabrication of CNTTFTs to achieve better electrical performances [4,9,11].

Now a days, researchers are fabricating CNTTFTs of different gate structures on flexible substrates like polyimide, polyethylene terephthalate (PET), polyethersulfone (PES), plastic transparency films, polyethylene naphthalate (PEN) to use in flexible applications such as radio frequency identification tags, electronic papers, digital circuits, smart skins, fingerprint scanners, photovoltaics [12-19]. CNTTFTs which exhibit stability on exposure to air after some days following fabrication, lower threshold voltages and lower subthreshold swing are suited in the circuits such as driving circuits of flexible displays and other digital circuits. The electrical characteristics comparison of flexible CNTTFTs with different gate structures is required to decide the better gate structure to be used in flexible applications.

In this work, the top, bottom and dual-gate CNTTFTs on a polyimide substrate are fabricated using photolithography for patterning of electrodes and SWCNTs thin film in the channel area, and their electrical characteristics are compared. The stability of top and dual-gate CNTTFTs was investigated by performing electrical characterization immediately after the fabrication and exposure to air for 60 days following fabrication.

Fabrication Process

Bottom, top and dual-gate CNTTFTs were fabricated on a flexible polyimide substrate. Photolithography and lift-off process was used for patterning of electrodes and SWCNTs thin film between source and drain.

Steps of fabrication of bottom and dual-gate CNTTFTs are illustrated in figure 1(a-i). 6 masks were prepared to use in photolithography for patterning of source, drain and gate electrodes, gate dielectric oxides, and SWCNTs thin film.

Preparation of masks starts with the writing of layouts using Clewin layout editor version 2.8. Then layouts were written on the iron-oxide-coated mask plates by laser writer LW 405 using layouts in GDSII format.

Polyimide tape 5413M with silicone adhesive coated on the bottom side, of thickness 70µm, a width of 25.4mm and length of 40 mm was affixed on a silicon wafer. Polyimide substrate fixed on a Si wafer is

shown in figure 1(a). Then before lithography process polyimide substrate was preheated at 90^{o}C for 5 minutes.

The process flow for fabrication of bottom gate CNTTFTs are as follows. The positive photoresist (PPR) S1813 was spin coated on a polyimide substrate. Substrate was preheated at 90^{o}C for 3 minutes, and nitrogen was blown on a mask. Double-sided aligner DSA EVG 620 was used in the process of photolithography. Then the photoresist deposited on polyimide substrate was exposed to ultraviolet (UV) light for 8seconds. Polyimide substrate was kept in MF319 developer solution for 15 seconds to remove softened resists and developed PPR is shown in figure 1(b).

Titanium/gold (Ti/Au) bottom gate of metal of thickness 7/50nm was deposited by 4 target E-beam evaporator (4-TEBE) and patterned using photolithography is shown in figure 1(c). Hafnium dioxide (HfO_2) dielectric layer of 10nm thickness was deposited by radio frequency (RF) sputtering, patterned using photolithography and resulting cross-sectional view is shown in figure 1(d).

Next process was SWCNTs deposition on the HfO_2 to form a thin film of SWCNTs. SWCNTs solution obtained from Nano Integris Inc., USA was used for thin film deposition. The solution contained 99.99% semiconducting purity SWCNTs. The solution obtained was in the form of an aqueous surfactant solution with a concentration of 1.0 mg SWCNTs in 25 ml solution. To increase the density of nanotubes on silicon dioxide(SiO_2) surface, the SiO_2 surface was amino isopropyl triethoxysilane(APTES) [12,-14] functionalized.

The following procedure for APTES functionalization was followed. The polyimide substrate was immersed in sulphochromic acid for 2 minutes and then rinsed in deionized water thoroughly to create OH bonds and dried using nitrogen (N_2) gas. The polyimide substrate was heated for 1 hour at 120^{o}C and 10^{-2}mbar pressure. A solution containing 60micro liter of 3-aminoisopropyltriethoxysilane and 20 ml of isopropyl alcohol [IPA] was prepared. The polyimide substrate was immersed in this prepared solution for 15 minutes in argon ambient. The ambient was created in a chamber by filling argon as an inert gas to prevent the polymerization of APTES. Next, the polyimide substrate was rinsed in IPA and dried using Argon gas to complete the process of amino isopropyl triethoxysilanefunctionalization of the HfO_2 surface. Then the polyimide substrate was immersed in SWCNT solution for 30minutes. Toremove sodium dodecyl sulphate (SDS) residual on CNTs, polyimide substrate was rinsed in IPA, followed by a rinseofde-ionized (DI) water and dried with nitrogen gas.

Unwanted SWCNTs outside channel region were removed by oxygen (O_2) plasma etching. The photolithographic steps were used to protect SWCNTs in the channel region. The schematic view of SWCNTs thin film after patterning is shown in figure 1(e).

To realize source and drain contacts of CNTTFTs the palladium/gold (Pd/Au) of 8/20nm thickness was deposited by 4TEBE and patterned using photolithography. The resulting cross-sectional view is shown in figure 1(f). To define more substantial area source, drain, and gate electrode contact pads on polyimide substrate Ti/Au of thickness 7/50nm was deposited by RF sputtering, and a lift-off processremoved Ti/Au from unwanted regions. Resultant cross-sectional view of fabricated bottom-gate CNTTFT is shown in figure 1(g).

Dual-gate CNTTFTs were fabricated using two additional steps after the fabrication of bottom-gateCNTTFTs. For top-gate dielectric, SiO_2 of thickness 10nm was patterned using photolithography is shown in figure 1(h). The Ti/Au top-gate of thickness 7/50 nm was patterned using photolithography is shown in figure 1 (i).

The process flow for fabrication of bottom-gate CNTTFTs with SiO_2 as a gate dielectric is same as CNTTFTs fabrication using HfO_2 as a gate dielectric, except HfO_2 deposition and patterning, the SiO_2 was used as dielectric and patterned as shown in step 1(h). CNTTFTs fabricated are of channel length (L) varying from 3 to 100 µm and channel width (W) varying from 3 to 50 µm.

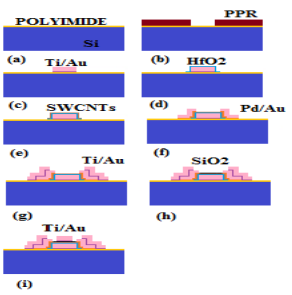

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Figure 1.Process stepsfor fabrication of bottom-gate and dual-gate CNTTFTs. (a) Polyimide substrate pasted on Si wafer. (b) Developed PPR. (c) Patterned Ti/Au gate. (d) Patterned gate dielectric HfO_2.(e) Patterned SWCNTs put on APTES functionalized HfO_2. (f) Patterned Pd/Au for source and a drain electrode (g) Patterned Ti/Au to formsubstantially significantspace source, drain and gate contact pads. (h) Patterned top gate dielectric SiO_2 of dual-gate CNTTFT.(i) Patterned top-gate metal Ti/Au of dual-gate CNTTFT.

Method of fabrication of top-gate CNTTFTs is shown in figure 2(a)-2(g). Polyimide tape 5413M with silicone adhesive coated on bottom side, of thickness 70µm, a width of 25.4mm and length of 40 mm was pasted on Si wafer of 2 inches. Polyimide substrate pasted on Si wafer was preheated at 90^{o}C for 5 minutes beforelithography process. HfO_2 of thickness 10nm deposited all over the polyimide substrate using RF sputtering as shown in figure 2.3(b). Subsequently, SWCNTs were placed to constitutea thin film of SWCNTs over the HfO_2 surface. The HfO_2 surface was APTES [16-18] functionalized prior to the SWCNTs deposition to increase the density of SWCNTs deposited.

The same procedure for APTES functionalization of the dielectric surface as that was followed in above mentioned bottom-gatefabrication process.

Unwanted SWCNTs outsidechannel region were depleted by O_2 plasma etching employing photolithographic methods to protect SWCNTs in a channel region is as given in figure 2.3(c). 4-TEBE depositedsource and drain electrodes were of metal Pd/Au of thickness 8/20nm. Placed metal Pd/Au was patterned by standard photolithography, and lift-off process is viewed in figure 2.3(d). The HfO_2 dielectric layer of 10nm thickness was placed by RF sputtering. Placed HfO_2 was patterned employing photolithography, and the resulting cross-sectional view is shown in figure 2.3(e). 4-TEBE deposited Ti/Au top-gate metal of thickness7/50nm. Ti/Au metal was patterned using photolithography is appeared in figure 2.3(f). More substantial area source, drain, and gate electrode contact pad regions of metal Ti/Au of thickness 7/50nm was deposited by RF sputtering on a polyimide substrate. Deposited metal Ti/Au was eliminated from undesiredareas by photolithography and lift-off process. Patterned more substantial area source, drain, and gate electrode contact pads of metal Ti/Au are shown in figure 2.3(g).

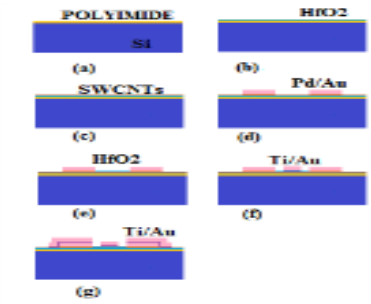

Figure 2.Process steps for fabrication of top-gate CNTTFTs. (a) Polyimide substrate pasted on the Si wafer.(b) HfO_2 deposited on a polyimide substrate.(c) SWCNTs placed on APTES functionalized HfO_2.(d) Patterned Pd/Au for source and drain electrode. (e) Patterned top-gate dielectric HfO_2. (f) Patterned Ti/Au gate.(g) Patterned Ti/ Au for extensive area source, drain and gate contact pads.

After the fabrication of CNTTFTs on a polyimide substrate the substrate was peeled-off from the Si wafer. After it was peeled off from Si wafer the photograph of polyimide substrate that was held with hands is shown in figure3.

Figure3.Polyimide substrate peeled-off from Si substrate after CNTTFTs fabrication.

Results and Discussion

In this sectiondiscussion on images of SWCNTs deposited taken by field emission scanning electron microscope (FESEM), Raman spectroscopy data of SWCNTs thin-film deposited on gate oxideand the study of comparison of electrical characteristics, electrical parameters such as maximum on current (I_{ON}) on-off current ratio (I_{ON}/I_{OFF}), transconductance (g_m),drain conductance (g_{ds}), carrier mobility (μ_{carr}) and threshold voltage (V_{th}) of flexible top, bottom and dual-gate CNTTFTs.Also, the investigation on the stability of

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flexible top and dual-gate CNTTFTs, when exposed to air fora time duration of 60 days after the fabrication wasdone.

FESEM image was taken tofind the density of SWCNTs placed on a polyimide substrate hasappeared in figure4.The density of SWCNTs deposited is around 70nanotubes/μm^2. Raman spectroscopy data was used to evaluate semiconducting purity of SWCNTs and to find whether the presence of metallic nanotubes is lower or higher [20]. Radial breadth modes (RBM) first-order and second-order Raman frequencies (150-350cm^{-1}) provide the data of diameter, chirality, and phonon structure. Graphene plane graphite band (1565–1595 cm^{-1}) gives dataof carbon-carbon stretching. The RBM and G-modes remain affected by diameter. Raman spectra of SWCNTs deposited on APTES functionalized SiO_2 dielectric surface have appeared in figure 5. The tops of radial breathing modes, the disordered band (D band), graphite band (G band) and G'band are shown in figure 5.RBM regions of SWCNTs provide qualitative proof of a relative population of semiconductive to metallic nanotubes put over the surface. Raman peaks at about 160–200cm^{-1} and 200–280 cm^{-1} are due to semiconducting and metallic SWCNTs respectively [21]. Raman spectroscopy RBM data shows peaks at a Raman shift less than 200cm^{-1}which demonstrates the highest semiconducting purity of SWCNTs and absence of metallic nanotubes in SWCNTs. Microscopic pictures of the flexible top-gate CNTTFTs fabricated on a polyimide substrate are shown in figure 6. Microscopic image of a fabricated flexible top-gateCNTTFT of L=5µm, W=40µm is shown in figure7.

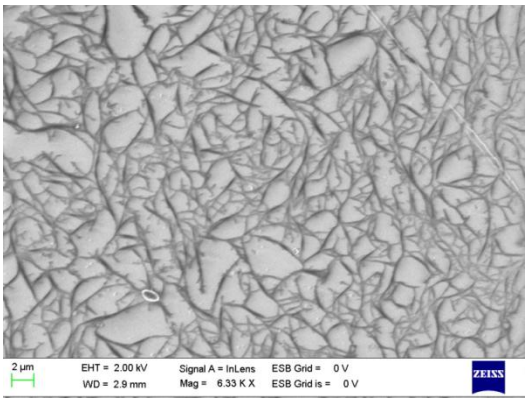

Figure4. FESEM image of a thin-film of SWCNTs deposited between electrodes of CNTTFTs on a polyimide substrate to form a channel.

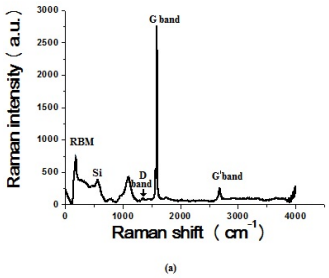

Figure5.Raman spectroscopy data of placed SWCNTs thin film.

Figure6.The microscopic pictureof a flexible top-gate CNTTFTs.

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Figure7.Microscopepicture of a fabricated flexible top-gate CNTTFT of L=5µm, W=40 µm.

Output and transfer characteristics of dual, bottom and top-gate flexible CNTTFT of L=8µm, W=5µm are shown in figure 8. Gate dielectrics employed in dual-gate flexible CNTTFTs are HfO_2 and $SiO_2$of thickness 40nm each, whereas top-gate and bottom-gate flexible CNTTFTs employs HfO_2 of thickness 40nm Output characteristics taken by the varying drain to source voltage (V_{DS}) at constant gate voltages (V_{GS}) are shown in figures8(a), 8(b), 8(c) correspondingly for dual, bottom and top-gate CNTTFTs. Dual-gate CNTTFTs showed p-type characteristics as shown in figure 8(a). Dual-gate CNTTFT has shown maximum on current of 63.9µA at constant V_{GS}= -50 V. The saturation voltage is reached at a voltage V_{DS}= -42V for a constant voltage of V_{GS}=-50V. Estimated drain conductance for a device at V_{GS}= -20V is 0.96µS. Topand bottom-gate CNTTFTs also presented p-type features asviewed from figures 8(c) and 8 (e).

Bottom-gate CNTTFT has showna peak on current of 30.7µA at constant V_{GS}= -50V. The saturation voltage is attained at a voltage V_{DS}= -40V for a constant voltage of V_{GS}= -50 V. Estimated drain conductance for a CNTTFT at V_{GS}= -20V is 1.02µS as viewed from figure8(c).

The top-gate CNTTFT has displayedpeak on current of 17.2µA at constant V_{GS}= -50V. The saturation voltage is reached at a voltage V_{DS}= -39V for a constant voltage of V_{GS}=--50 V. Estimated drain conductance for a CNTTFT at V_{GS}= -20V is 1.1µS as seen from figure 8(e).

Study of output characteristics of flexible CNTTFTs of various gate arrangementsconfirmed that dual–gate CNTTFTs have a higher peak on current and less value of drain conductance than bottom-gate and top-gate CNTTFTs because of the better control of the channel than other two. Between flexible bottom and top-gate CNTTFTs, flexible bottom-gate CNTTFTs havedisplayed a higher amount of peak on current and weaker drain conductance.

The carrier mobility is calculated applying equation (1)

$$\mu_{carr}=Lg_m/V_{DS}C_{ox}W \quad (1)$$

where $C_{ox}$is the gate capacitance per unit area determined consideringinto account electrostatic coupling among nanotubes and utilizing formula reported in[22-24].

The transfer characteristics for various voltages V_{GS} of dual, bottomand top-gate CNTTFTs of L=8µm, W=5µm correspondingly aregiven in figures 8(b), 8(e), 8(b), respectively. On current from the transfer characteristics of dual-gate CNTTFT as seenfrom figure 8(b) is 27.2 µA at constant V_{DS}= -20V. At constant V_{DS} of -20 V obtained values of on-off current ratio, transconductance, subthreshold swing, threshold voltage and mobility of dual-gate CNTTFT correspondingly are $9.65X10^4$, 0.6 µS, 172.08mV/decade, -1V and $0.2136cm^2/Vs$.

On current estimated from transfer characteristics of bottom-gate CNTTFT is shown in figure 8(d) is 13.1 µA at constant V_{DS}= -20V.At constant of V_{DS} of -20 V deduced values of on-off current ratio, transconductance, subthreshold swing, threshold voltage and mobility of bottom-gate CNTTFT correspondingly are $1.6375X10^4$, 0.20µS, 321.54 mV/decade,-2V and 0.08667 cm^2/Vs.

On current from transfer characteristics of top-gate CNTTFT is viewed in figure 8(f) is 5.08µA at constant V_{DS}= -25V.

At constant $V_{DS}$of -25 V the deduced values of on-off current ratio, transconductance, subthreshold swing, threshold voltage and mobility of top-gate CNTTFT correspondingly are $1.668X10^3$, 0.20µS, 321.54 mV/decade,-2.5V and 0.1414 cm^2/Vs.

Dual-gate CNTTFT has displayed better steep subthreshold swing, higher on-off current ratio, better transconductance contrasted to the top and bottom-gate CNTTFTs. Dual-gate CNTTFTssurpassed single-gate CNTTFTs in electrical performance because of the higherauthority of channel area between the source and drain electrodes since dual-gate devices have two gates.

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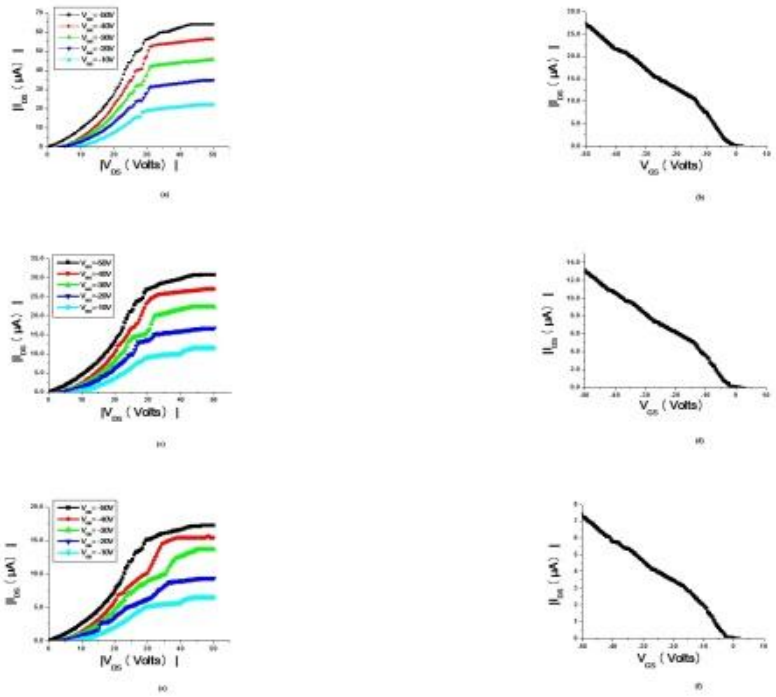

Figure8. Output and transfer characteristics of flexible CNTTFT of channel length equal to 8µm, channel width equal to5µm for various gate arrangements. Output characteristicsof(a)Dual-gate. (c) Bottom-gate. (e) Top-gate. Transfer characteristics of (b) Dual-gate.(d) Bottom-gate. (f) Top-gate.

Stability as a function of time after the fabrication of CNTTTFTs is studied for dual-gate flexible CNTTFT of L=15µm, W=5µm.Transfer characteristics of dual-gate flexible CNTTFT plotted immediately after fabrication and exposure to air for60 days later fabrication is presented in figure9. Other than threshold voltageelectrical performance of flexible CNTTFT is not degraded significantly.The shift in threshold voltage shift is 1.3V. Degradation of electrical performance parameters is not displayed because of encapsulation of SWCNTs thin-film by two gatesto air.

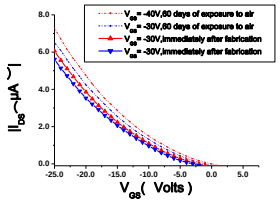

Figure 9. Transfer characteristics of flexible dual-gate CNTTFT of L=15µm, W=5µm measured immediately after the fabrication and exposure to air for 60 days after the fabrication.

Stability as a function of time after the fabrication of CNTTTFTs is studied for top-gate flexible CNTTFT of L=5µm, W=5µm.Transfer characteristics of top-gate flexible CNTTFT plotted immediately after fabrication and exposure to air for60 days later fabrication is presented in figure10. Other than threshold voltage electrical performance of flexible CNTTFT is not degraded significantly.The shift in threshold voltage shift is 1V. Degradation of electrical performance parameters is not displayed because of encapsulation of SWCNTs thin-film by a gatetoair.

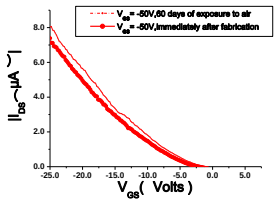

Figure 10. Transfer characteristics of flexible top-gate CNTTFT of L=5µm, W=5µm measured immediately after the fabrication and exposure to air for 60 days after the fabrication.

When compared to the dual-gate flexible CNTTFTs shift in threshold voltage of top-gate flexible CNTTFTs is lesser because the area of SWCNTs thin-film exposed in the gaps separating gate structure, andsource and drain electrodes is lesser since it is a single gate.

Stability as a function of timeafter the fabrication of CNTTTFTs exhibitsno significant degradation in electrical performance is displayed by both dual-gate and top-gate flexible CNTTFTs but exhibited a threshold shift of lesser than 1.3V.

Conclusion

In the present work, top, bottom and dual-gate carbon nanotube thin film transistors ofvarious dimensions with single-walled carbon nanotubes of 99.99% semiconducting purity on a polyimide substrate were fabricated. Electrical performance of flexible CNTTFTs with various gate arrangementswas compared. Top, bottom, and dual-gate CNTTFTs showed p-type performance. Dual-gate CNTTFTs bettered the bottom and top-gate CNTTFTs of identicaldimensions in on-off current ratio, transconductance, drain conductance, subthreshold slope and mobility. Dual and top-gate CNTTFTs shown threshold shift of less than 1.3V and stable in rest of electrical performance parameters other than threshold voltage without much variation when exposed to airfor 60 days later fabrication.Present work investigated that dual-gate CNTTFTs exhibited better electrical performances and gate control over channel than top and bottom -gate CNTTFTs. The dual-gate CNTTFTs are preferred for better electrical performances than top and bottom-gate inflexible uses.

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